We claim:

1. An oscillator with improved sensitivity to component variation due to process shift, comprising:

a first comparator circuit and a second comparator circuit;

a charging-discharging circuit coupled to a first input of the first comparator circuit and to a first input of the second comparator circuit;

a resistor string coupled to a second input of the first comparator circuit and to a second input of the second comparator circuit;

a latch configured to combine an output of the first comparator circuit and an output of the second comparator circuit;

wherein the resistor string is operable to maintain a first reference voltage at the second input of the first comparator circuit and a second reference voltage at the second input of the second comparator circuit;

wherein the first reference voltage is substantially higher than the second reference voltage;

wherein an output of the latch is coupled to the charging-discharging circuit, forming a feedback loop;

wherein the output of the first comparator circuit is operable to change states when the first input of the first comparator circuit reaches a voltage level substantially commensurate with the first reference voltage;

wherein the output of the second comparator circuit is operable to change states when the first input of the second comparator circuit reaches a voltage level substantially commensurate with the second reference voltage;

wherein the charging-discharging circuit is operable to charge the first input of the first comparator circuit and the first input of the second comparator circuit to a voltage level substantially commensurate with the first reference voltage;

wherein the charging-discharging circuit is operable to discharge the first input of the first comparator circuit and the first input of the second comparator circuit to a voltage level substantially commensurate with the second reference voltage; and

wherein the resistor string comprises at least two different structure types.

2. The oscillator of claim 1, wherein the charging-discharging circuit comprises:

a resistance; and

a capacitance coupled to the resistance;

wherein the resistance and the capacitance are configured together to substantially determine a time period of oscillation of the oscillator.

3. The oscillator of claim 2, wherein the resistance comprises at least two different structure types.

4. The oscillator of claim 3, wherein a first of the at least two different structure types comprises poly-silicon, and a second of the at least two different structure types comprises n+ diffusion.

5. The oscillator of claim 2;

wherein the first input of the first comparator circuit and the first input of the second comparator circuit are both coupled to a first terminal of the capacitance; and

wherein a second terminal of the capacitance is coupled to a common ground.

6. The oscillator of claim 1, wherein the resistor string comprises a first resistance, a second resistance, and a third resistance;

wherein the first resistance couples a power supply to the second input of the first comparator circuit;

wherein the second resistance couples the second input of the first comparator circuit to the second input of the second comparator circuit;

wherein the third resistance couples the second input of the second comparator circuit to a common ground; and

wherein the first resistance comprises a first structure type, the second resistance comprises a second structure type different from the first structure type, and the third resistance comprises the first structure type and the second structure type.

7. The oscillator of claim 6;

wherein a nominal value of the first resistance, a nominal value of the second resistance and a nominal value of the third resistance are substantially equivalent to each other.

8. The oscillator of claim 1, wherein the latch comprises an SR-latch.

9. The oscillator of claim 1, wherein a first of the at least two different structure types comprises poly-silicon, and a second of the at least two different structure types comprises n+ diffusion.

10. An oscillator with improved sensitivity to component variation due to process shift, comprising:

a first comparator circuit and a second comparator circuit;

a resistor string coupled to a second input of the first comparator circuit and to a second input of the second comparator circuit;

a latch configured to combine an output of the first comparator circuit and an output of the second comparator circuit;

a resistance coupling an output of the latch to a first input of the first comparator circuit and to a first input of the second comparator circuit;

a capacitance coupling a common ground to the first input of the first comparator circuit and to the first input of the second comparator circuit;

wherein the resistor string is operable to maintain a first reference voltage at the second input of the first comparator circuit and a second reference voltage at the second input of the second comparator circuit;

wherein the first reference voltage is substantially higher than the second reference voltage;

wherein the output of the first comparator circuit is operable to change states when the first input of the first comparator circuit reaches a voltage level substantially commensurate with the first reference voltage;

wherein the output of the second comparator circuit is operable to change states when the first input of the second comparator circuit reaches a voltage level substantially commensurate with the second reference voltage; and

wherein the resistance comprises at least two different structure types.

11. The oscillator of claim 10, wherein the resistor string comprises a first resistance, a second resistance, and a third resistance;

wherein the first resistance couples a power supply to the second input of the first comparator circuit;

wherein the second resistance couples the second input of the first comparator circuit to the second input of the second comparator circuit; and

wherein the third resistance couples the second input of the second comparator circuit to a common ground.

12. The oscillator of claim 11, wherein the first resistance comprises a first structure type, the second resistance comprises a second structure type different from the first structure type, and the third resistance comprises the first structure type and the second structure type.

13. The oscillator of claim 11;

wherein a nominal value of the first resistance, a nominal value of the second resistance and a nominal value of the third resistance are substantially equivalent to each other.

14. The oscillator of claim 10, wherein the latch comprises an SR-latch.

15. The oscillator of claim 10, wherein a first of the at least two different structure types comprises poly-silicon, and a second of the at least two different structure types comprises n+ diffusion.

16. A method for implementing an integrated oscillator with improved sensitivity to component variation due to process shift, the method comprising:

forming a first resistance of a first structure type;

forming a second resistance of a second structure type, wherein the second structure type is different from the first structure type;

forming a third resistance, wherein the third resistance comprises a first resistor of the first structure type and a second resistor of the second structure type;

coupling a supply voltage to a first input of a first comparator circuit through the first resistance;

coupling the first input of the first comparator circuit to a first input of a second comparator circuit through the second resistance;

coupling the first input of the second comparator circuit to a common ground through the third resistance;

coupling an output of the first comparator circuit and an output of the second comparator circuit to a latch;

coupling an output of the latch to a second input of the first comparator circuit and to a second input of the second comparator circuit through a charge-discharge circuit; and

providing the output of the latch as output of the integrated oscillator.

17. The method of claim 16, wherein the latch comprises an SR-latch.

18. The method of claim 16, wherein said coupling the output of the latch comprises:

coupling the output of the latch to a first terminal of a fourth resistance;

coupling a first terminal of a capacitance to a second terminal of the fourth resistance, to the second input of the first comparator circuit, and to the second input of the second comparator circuit; and

coupling a second terminal of the capacitance to the common ground.

19. The method of claim 16, wherein the first structure type comprises poly-silicon, and the second structure type comprises n+ diffusion.

20. The method of claim 16, wherein a nominal value of the first resistance, a nominal value of the second resistance and a nominal value of the third resistance are substantially equivalent to each other.

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